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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. FIS920010253US1

In Re Application Of:

Darren L. Anand et al.

Serial No.	Filing Date	Examiner	Group Art Unit
10/026,118	December 21, 2001	Ly D. Pham	2818

Invention:

FLEXIBLE MULTIBANKING INTERFACE FOR EMBEDDED MEMORY APPLICATIONS

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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Steven Capella

Signature

Dated: 9/18/03

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I certify that this document and fee is being deposited on 9/18/03 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Karen Cinq-Mars 9/18/03

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Karen Cinq-Mars

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Karen Cinq-Mars 9/18/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit 2818

In re application of	:	September 18, 2003
Darren L. Anand et al.	:	Examiner: Ly D. Pham
Serial No. : 10/026,118	:	
Filed: December 21, 2001	:	IBM Corporation Dept. 18G/Bldg, 300-482
Title: FLEXIBLE MULTIBANKING INTERFACE FOR EMBEDDED MEMORY APPLICATIONS	: : :	2070 Route 52 Hopewell Junction, NY 12533-6531

APPEAL BRIEF

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final Rejection of claims 1-16. A correct copy of the claims is attached in the Appendix.

Real Party in Interest

The real parties in interest is International Business Machines Corporation per an assignment recorded in the US Patent and Trademark Office at Reel/Frame: 012408/0880 on December 21, 2001.

Related Appeals and Interferences

None.

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Status of Claims

Claims 1-16 are pending.

Status of Amendments

No amendments after Final Rejection have been submitted.

Summary of Invention

The invention centers on an improved interface for multibank embedded DRAM macro that enables a high performance, easily grown embedded DRAM macro. The macro is characterized by independently accessible banks, each with a dedicated bank select, as well as dedicated row decoder and dedicated redundancy. The interface of the invention has advantages over typical synchronous DRAM interfaces in that operations to each bank are independent. The multi-bank interface of the invention extends the macro performance by allowing concurrent operations to independent banks and thereby allowing improved bus utilization during multi-bank operations. See the specification at page 4, lines 3-14.

Issues

1. Whether claims 1, 4, 6, 8, 9, 12, 14 and 16 are patentable under 35 USC 102(e) over Dono et al. (US Pat. Pub 2002/0015328 A1).

2. Whether claims 2-3 and 10-11 are patentable under 35 USC 103(a) over Dono et al. (US Pat. Pub 2002/0015328 A1) in view of Yamaguchi (US Pat. 6067632).

3. Whether claims 5 and 13 are patentable under 35 USC 103(a) over Dono et al. (US Pat. Pub 2002/0015328 A1) in view of Jeddeloh et al. (US Pat. 6430742).

4. Whether claims 7 and 15 are patentable under 35 USC 103(a) over Dono et al. (US Pat. Pub 2002/0015328 A1).

Grouping of Claims

The claims stand or fall together within each respective issue identified above.

Argument

1. Whether claims 1, 4, 6, 8, 9, 12, 14 and 16 are patentable under 35 USC 102(e) over Dono et al. (US Pat. Pub 2002/0015328 A1).

Dono et al. discloses a DRAM design for a memory chip, not a macro for an embedded DRAM. Dono et al. discloses the use of redundancy in a DRAM device, however, it is not clear that such redundancy is embedded in each bank. Dono et al. does not disclose or suggest the use of a dedicated row decoder for each bank, nor independent bank selects. Appellants submit that Dono et al. decodes the bank address and sends one bank selection signal. See for example Figure 1. There is no indication of multiple signals running simultaneously to multiple banks.

2. Whether claims 2-3 and 10-11 are patentable under 35 USC 103(a) over Dono et al. (US Pat. Pub 2002/0015328 A1) in view of Yamaguchi (US Pat. 6067632).

Dono et al. discloses a DRAM design for a memory chip, not a macro for an embedded DRAM. Dono et al. discloses the use of redundancy in a DRAM device, however, it is not clear that such redundancy is embedded in each bank. Dono et al. does not disclose or suggest the use of a dedicated row decoder for

each bank, nor independent bank selects. Appellants submit that Dono et al. decodes the bank address and sends one bank selection signal. See for example Figure 1. There is no indication of multiple signals running simultaneously to multiple banks.

Yamaguchi discloses a design where the column access signal is latched to a master flip-flop. It is not apparent that Yamaguchi discloses latching of independent bank selects to a master. Further, Yamaguchi does not disclose or suggest the other aspects of the invention which Dono et al. fails to suggest as noted above, especially the independent bank selects.

3. Whether claims 5 and 13 are patentable under 35 USC 103(a) over Dono et al. (US Pat. Pub 2002/0015328 A1) in view of Jeddeloh et al. (US Pat. 6430742).

Dono et al. discloses a DRAM design for a memory chip, not a macro for an embedded DRAM. Dono et al. discloses the use of redundancy in a DRAM device, however, it is not clear that such redundancy is embedded in each bank. Dono et al. does not disclose or suggest the use of a dedicated row decoder for each bank, nor independent bank selects. Appellants submit that Dono et al. decodes the bank address and sends one bank selection signal. See for example Figure 1. There is no indication of multiple signals running simultaneously to multiple banks.

Jeddeloh et al. discloses that many DRAM designs are capable of operating in page mode. Further, Jeddeloh et al. does not disclose or suggest the other aspects of the invention which Dono et al. fails to suggest as noted above, especially the independent bank selects.

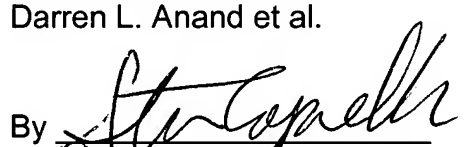
4. Whether claims 7 and 15 are patentable under 35 USC 103(a) over Dono et al. (US Pat. Pub 2002/0015328 A1).

Dono et al. discloses a DRAM design for a memory chip, not a macro for an embedded DRAM. Dono et al. discloses the use of redundancy in a DRAM device, however, it is not clear that such redundancy is embedded in each bank. Dono et al. does not disclose or suggest the use of a dedicated row decoder for each bank, nor independent bank selects. Appellants submit that Dono et al. decodes the bank address and sends one bank selection signal. See for example Figure 1. There is no indication of multiple signals running simultaneously to multiple banks.

Conclusion

Based on the above arguments, appellants submit that the present claims are patentable over the prior art of record that all the rejections should be reversed.

Respectfully submitted,
Darren L. Anand et al.

By 
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Appendix

Claims on Appeal

1. A multibank DRAM macro, said macro comprising:
   (a) a plurality of DRAM memory banks, each bank respectively comprising:
      (i) an array of DRAM memory cells,
      (ii) bitlines and wordlines, respectively defining columns and rows of the array,
      (iii) a dedicated row address decoder circuit,
      (iv) a column address decoder circuit,
      (v) dedicated spare rows and columns for redundancy,
   (b) a dedicated bank select input for each respective bank, each bank input controlling operation of its respective bank, and
   (c) a data path receiver / driver shared by at least two banks.

2. The DRAM macro of claim 1 further comprising (d) a master select input.

3. The DRAM macro of claim 2 wherein said bank select inputs are latched to a falling edge of a signal from said master select input.

4. The DRAM macro of claim 1 wherein said macro further comprises a write enable input.

5. The DRAM macro of claim 1 wherein said macro further comprises a page mode select input.

6. The DRAM macro of claim 1 wherein each bank further comprises (vi) at least one sense amplifier.

7. The DRAM macro of claim 1 wherein each bank has capacity for about 1 Mb of data.

8. The DRAM macro of claim 7 wherein said macro comprises at least 4 of said banks.

9. An integrated circuit device comprising a logic core and a DRAM macro wherein said DRAM macro is a multibank DRAM macro comprising:
   (a) a plurality of DRAM memory banks, each bank respectively comprising:
      (i) an array of DRAM memory cells,
      (ii) bitlines and wordlines, respectively defining columns and rows of the array,
      (iii) a dedicated row address decoder circuit,
      (iv) a column address decoder circuit ,
      (v) dedicated spare rows and columns for redundancy,
   (b) a dedicated bank select input for each respective bank, each bank input controlling operation of its respective bank, and
   (c) a data path receiver / driver shared by at least two banks.

10. The integrated circuit device of claim 9 wherein said DRAM macro further comprises (d) a master select input.

11. The integrated circuit device of claim 10 wherein said bank select inputs are latched to a falling edge of a signal from said master select input.

12. The integrated circuit device of claim 9 wherein said DRAM macro further comprises a write enable input.

13. The integrated circuit device of claim 9 wherein said DRAM macro further comprises a page mode select input.

14. The integrated circuit device of claim 9 wherein each bank of said DRAM macro further comprises (vi) at least one sense amplifier.

15. The integrated circuit device of claim 9 wherein each bank of said DRAM macro has capacity for about 1 Mb of data.

16. The integrated circuit device of claim 15 wherein said DRAM macro comprises at least 4 of said banks.

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